PREPARED BY: DATE	S H A R P	SPEC No. LC96608
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APPROVED BY: DATE	LIQUID CRYSTAL DISPLAY GROUP SHARP CORPORATION	PAGE 24 Pages
		APPLICABLE DIVISION
	S P E C I F I C A T I O N	■ DUTY PANEL DEVELOPMENT CENTER ❑ ITFT DEVELOPMENT CENTER ❑ ILCD PRODUCTS DEVELOPMENT CENTER ❑ IEL PRODUCTION DEPT.

Device specification for Passive Matrix LCD module

Model No.

LM64P89L

❑ iCUSTOMER'S APPROVAL

DATE

PRESENTED BY

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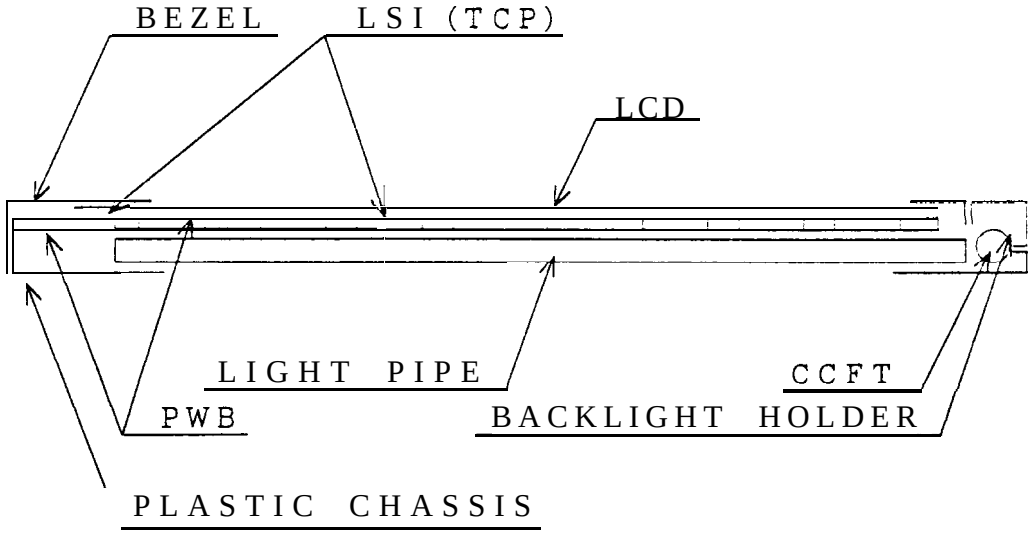
LCD GROUP

1. Application

This data sheet is to introduce the specification of LM64P89L,Passive Matrix type LCD Module

2. Construction and Outline

Construction:640×480 dots display unit consisting of an LCD panel, PWB(printed wiring board) with electric components mounted onto,TCP(tape carrier Package) to connect the LCD panel and PWB electrically, and plastic chassis with CCFT backlight and bezels to fix them mechanically.



Outline : See Fig. 10

Connection : See Fig. 10 and Table 6

3. Mechanical Specif cations

Table 1

Parameter	Specifications	Module
Outline dimensions	268 (W) × 190 (H) × 7MAX(D)*1	mm
Effective viewing Area	215.2 (W) X162.4 (H)	mm
Display format	640(W) X480(H) full dot	
Dot-size	0.30 × 0.30	mm
Dot spacing	0.03	mm
*2 Dot color	Black *3	
*2 Background color	White *3	
Weight	Approx. 340	g

*1 Excluded the mounting tabs.

*2 Due to the characteristics of the LC material, the colors vary with environmental temperature.

*3 Positive-type display

Displayed data "H": Dots ON : Black

Displayed data "L": Dots OFF: White

4. Absolute Maximum Ratings

4-1 Electrical absolute maximum ratings

Table 2

Parameter	Symbol	MIN.	MAX.	Unit	Remark
Supply voltage (Logic)	V_{DD}-V_{SS}	0	6.0	V	Ta=25 "C
Supply voltage (LCD drive)	V_{DD}-V_{EE}	0	30.0	V	Ta=25 "C
Input voltage	V_{IN}	0	V_{DD}	V	Ta=25 °C

4-2 Environmental Condit ons

Table 3

I tern	Tstg		Topr		Remark
	MIN.	MAX.	MIN.	MAX.	
Ambient temperatuer	-25 "C	+60 "C	O "C	+45 "C	Note 4
Humidity	Note I		Note 1		No condensation
Vibration	Note 2		Note 2		3 directions (X/Y/Z)
Shock	Note 3		Note 3		6 directions (±X±Y±Z)

Note 1) Ta≦40 "C . . . ..95 % RH Max

Ta>40 "C..... Absolute humidity shall be less than Ta=40 "C/95 % RH.

Note 2) These test condition are in accordance with "IEC 68-2-6".

Frequency	10 Hz～57 Hz	57 Hz～500 Hz
Vibration level	–	9.8 m/s² (1 G)
Vibration width	0.075 mm	–
I Interval	5 Hz～500 Hz～5 Hz/11 min	

2 hours for each direction of X/Y/Z (6 hours as total)

Note 3) Accerelation : 490 m/s²

Pulse width : 11 ms

3 times for each direction of ±X／±Y／±Z

Note 4) Care should be taken so that the LCD Module may not be subjected to the temperature out of this specification.

5. Electrical Specifications

5-1 Electrical characteristics

Tabel 4 Ta=25 "C

Parameter	Symbol	Conditions	Min.	TYP.	Max.	Unit
SupPlY voltage (Logic)	V_{DD}-V_{SS}	Note 1) Note 2)	4.75	5.0	5.5	V
Supply voltage (LCD drive)	V_{DD}-V_{EE}	Vote 3)Note 4)Note 5	20.1	23.9	28.2	V
Input signal voltage	V_{IN}	"H" level	0.8 V_{DD}		V_{DD}	v
		"L" level	0	-	0.2 V_{DD}	v
Input leakage current	I_{IL}	"H" level	—	—	250	μA
		"L" level	-250	—	—	μA
Supply current (Logic)	I_{DD}	Note 6)	—	24	36	mA
SUPPLY currect (LCD dirve)	I_{EE}		—	17	26	mA
Power consumption	Pd		—	450	680	mW

Note 1) V_{DD} to be applied according to the specifications shall be regulated and sudden fluctuation of V_{DD}, even if the fluctuation is within the specifications, shall be strictly avoided.

Note 2) V_{SS} is ground potential.

Note 3) The viewing angle θ at which the optimum contrast is obtained by adjusting V_{EE}-V_{SS}. Refer to Fig.4 for the definition of θ.

Note 4) Max. and Min. values are specified as the Max. and Min. voltage within the condition of operational temperature range (O-45 "C). TYP. values are specified as the typical voltage at 25 "C.

Note 5) V_{EE} is minus potential.

Note 6) Display high frequency pattern.

V_{DD} = 5 V, V_{DD}-V_{EE} = 23.9 V, Frame frequency = 85 Hz, Display pattern = 1 bit checker

display ■□■□■□■□■□■□■□■□■□■□■□■□■□■□

pattern □■□■□■□■□■□■□■□■□■□■□■□■□■

■ oaounMaMaMnmomnmn9uMaan

5-2 Input capacitance

Table 5

Signal	Input capacitance
s	40 PF TYP
CP1,DISP	250 PF TYP
CP2	200 pF TYP
DU0～DU3	200 pF TYP
DL0～DL3	200 pF TYP

5-3 Interface signals

Table 6

OLCD

Pin No	Symbol	Description	Level
1	s	Scan start-up signal	"H"
2	CP1	Input data latch signal	H→L
3	CP2	Data input clock signal	H→L
4	DISP	Display control signal	Display on ..''H" off..''L"-
5	VDD	Power supply for logic and LCD(+)	
6	Vss	Ground potential	
7	VEE	Power supply for LCD (-)	
8	DUO	Display data signal (Upper half)	H(ON),L(OFF)
9	DU1		
10	DU2		
11	DU3		
12	DLO	Display data signal (Lower half)	H(ON),L(OFF)
13	DL1		
14	DL2		
15	DL3		

○CCFT

Pin No	Symbol	Description	Level
1	GND	Ground line (from Inverter)	
2	NC		
3	NC		
4	HV	High voltage line(from Inverter)	

Note) Pin No. and its location are shown in Fig. 10.

OLCD

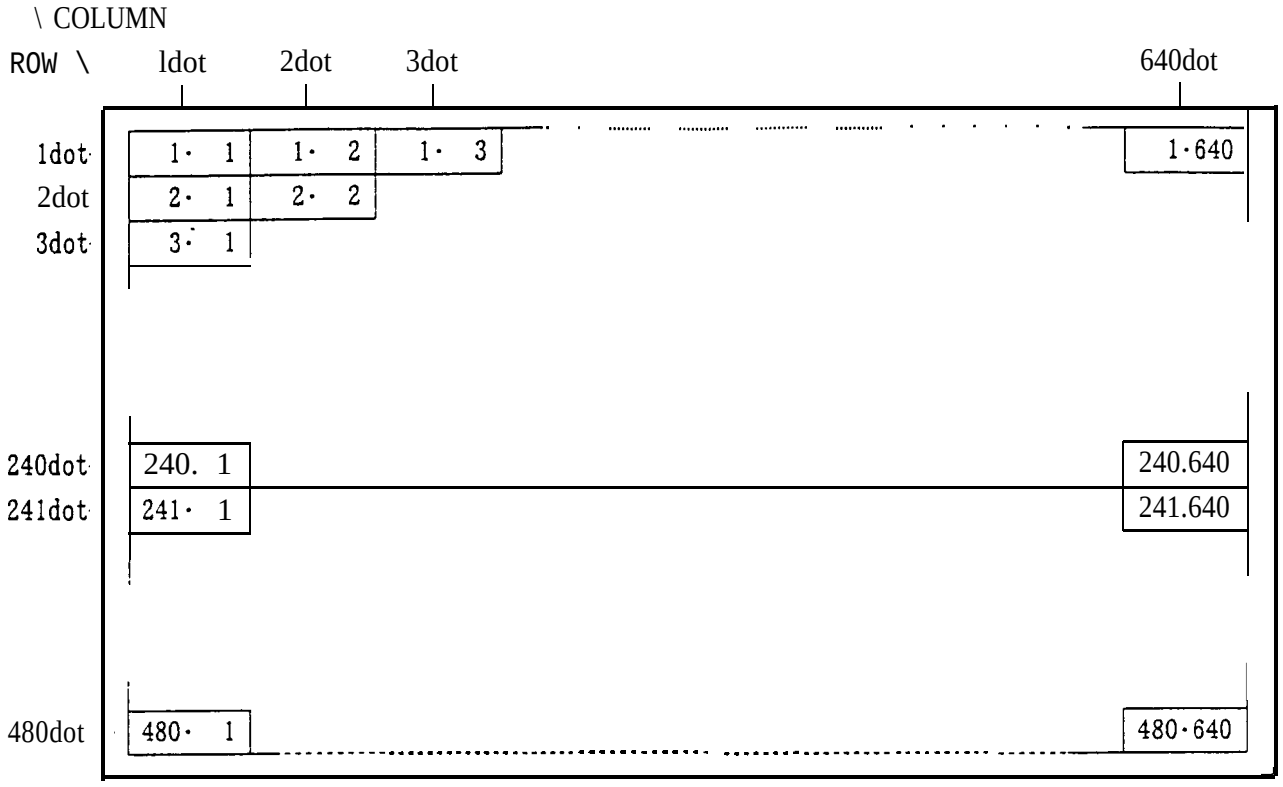
Used connector: 5326 -1510 MOLEX)

Mating connector: 5102 -1500 MOLEX)

OCCFT

Used connector: M63M83-04(MITSUMI)

Mating connector: M60-04-30-114P(MITSUMI)
M60-04-30-134P(MITSUMI)
M61M73-04(MITSUMI)



Note) 1·2 means 1st row 2nd column dot.

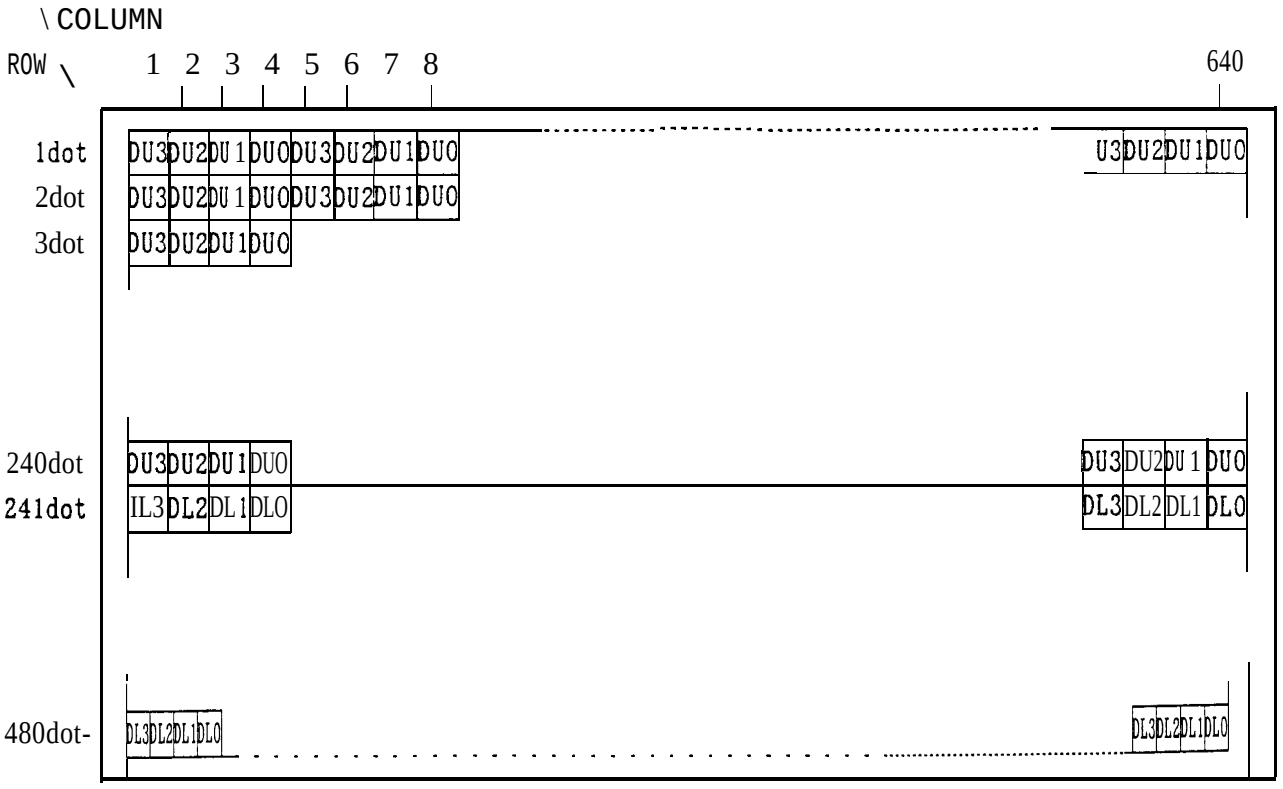


Fig. 1 Dot chart of display area

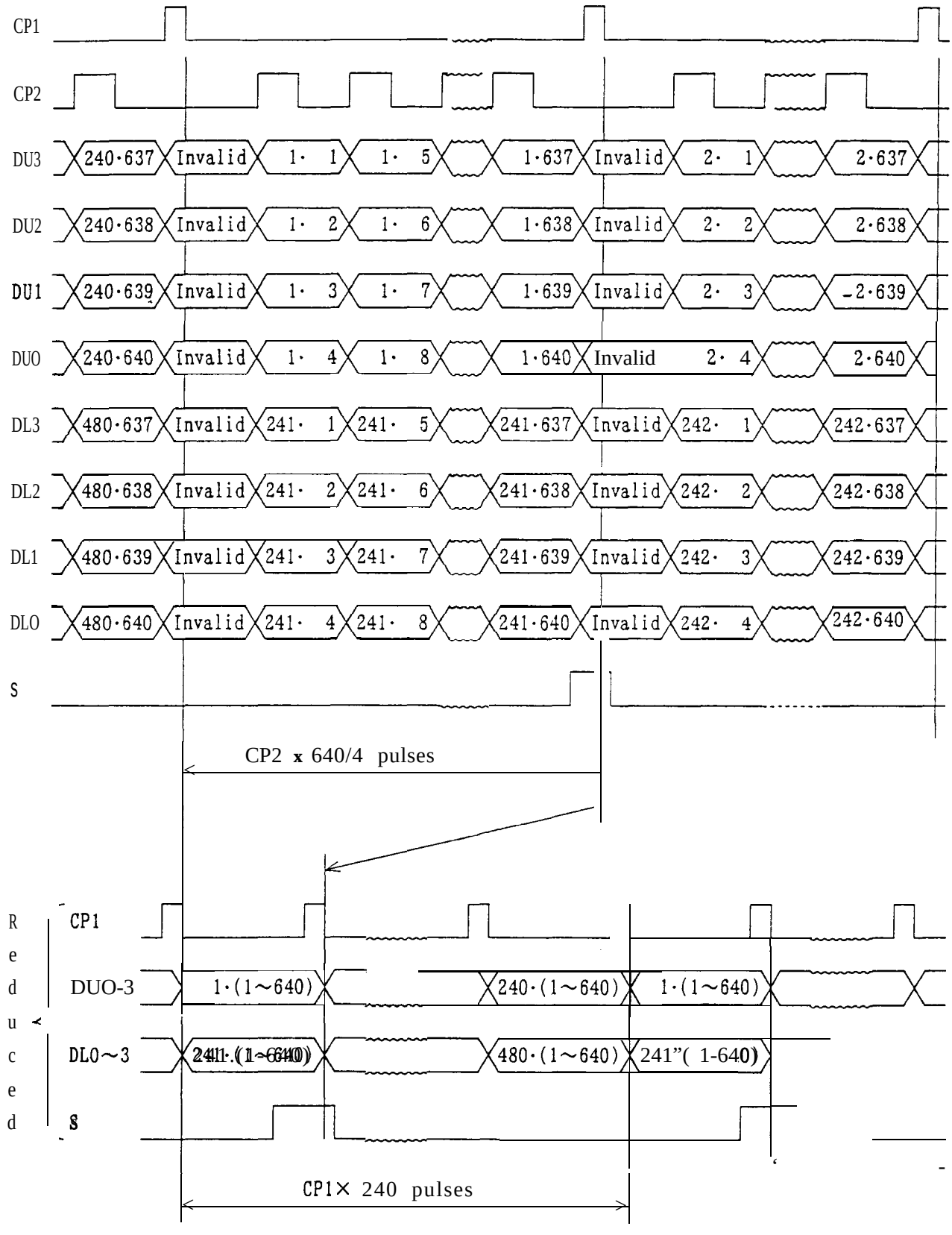
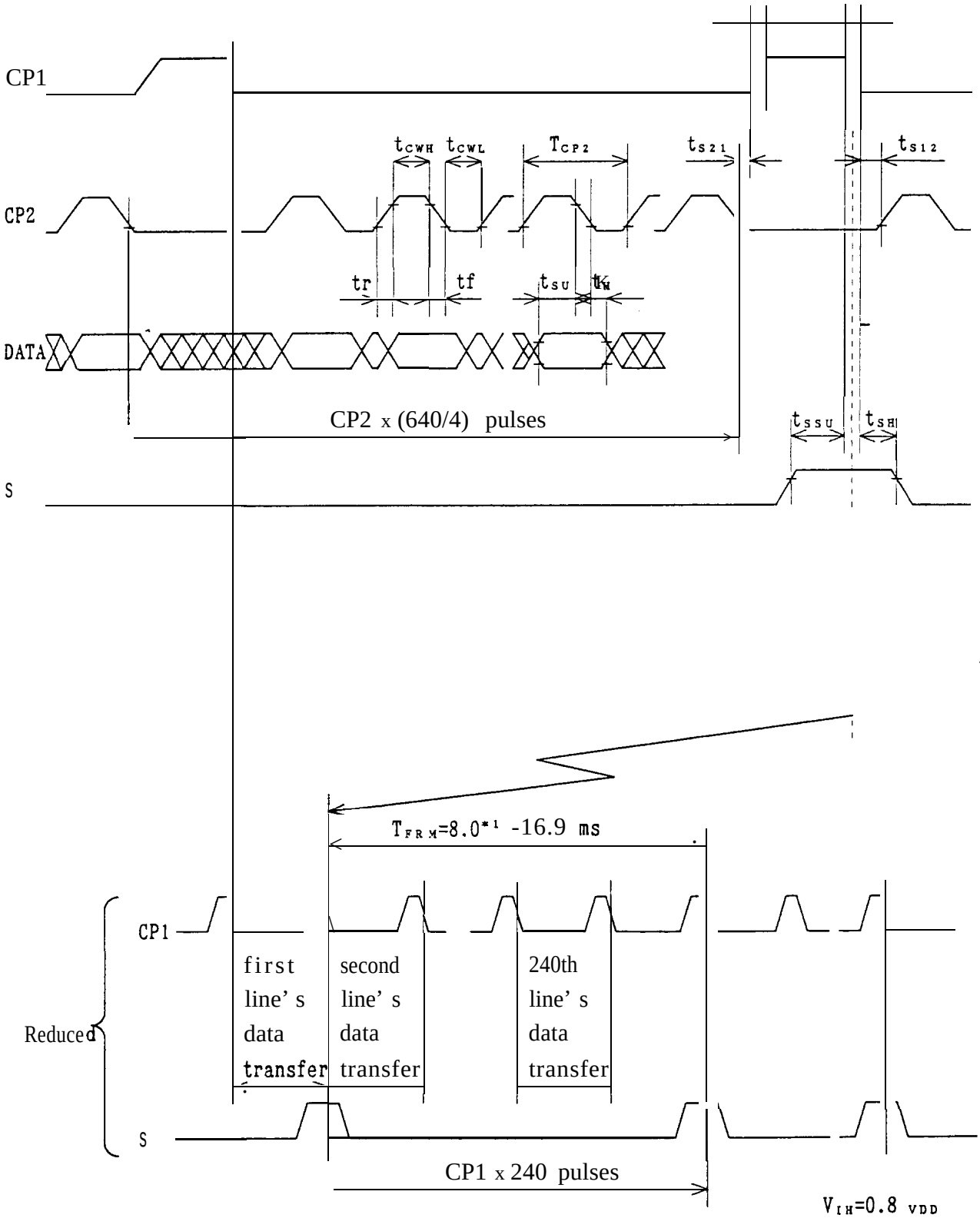


Fig.2 Data input timing



∗1 See table 7

Fig.3 Interface timing chart

Table 7 Interface timing ratings

Item	Symbo 1	Rating			Unit
		MIN.	TYP.	MAX.	
Frame cycle	T_{FRM}	8.0[81]		16.9	ms
CP2 clock cycle	T_{CP2}	152			ns
"H" level clock width	t_{CWH}	65			ns
"L" level clock width	t_{CWL}	〃 65			ns
"H" level latch clock width	t_{LWH}	70			ns
Data set up time	t_{SU}	50			ns
Data hold time	t_H	40			ns
S set up time	t_{SSU}	100			ns
S hold time	t_{SH}	100			ns
CP2↑ clock allowance time from CP1↓	t_{S21}	0			ns
CP1↑ clock allowance time from CP2↓	t_{S12}	0			ns
Clock rise/fall time	tr,tf			t_{rf}*2	ns

*1 : LCD Module functions at the minimum frame cycle of 8 ms (Maximum frame frequency of 125Hz). Owing to the characteristics of LCD Module, "shadowing" will become more eminent as frame frequency goes up, while flicker will be reduced.

According to our experiments, frame cycle of 11.7 ms Min. or frame frequency of 85 Hz Max. will demonstrate optimum display quality in terms of flicker and "shadowing". But since judgement of display quality is subjective and display quality such as "shadowing" is pattern dependent, it is recommended that decision of frame cycle or frame frequency, to which power consumption of the LCD Module is propotional,be made based on your own through testing on the LCD Module with every possible patterns displayed on it.

*2 : t_{rf} =50 in case $t_{CT}=(T_{CP2}-t_{CWH}-t_{CWL})/2 \geqq 50$

$t_{rf} = t_{CT}$ in case $t_{CT}=(T_{CP2}-t_{CWH}-t_{CWL})/2 < 50$

6. Module Driving Method

6.1 Circuit configuration

Fig.9 shows the block diagram of the Module's circuitry.

6.2 Display Face Configuration

The display face electrically consists of two (upper and lower) display segments so that the unit may offer higher contrast by reducing drive duty ratio. Each display segment (640x240 dots) is driven at 1/240 duty ratio.

6.3 Input Data and Control Signal

The LCD driver is 80 bits LSI, consisting of shift registers, latch circuits and LCD driver circuits.

Display data which are externally divided into data for each row (640dots) will be sequentially transferred in the form of 4-bit parallel data through shift registers by Clock Signal CP2 from the left top of the display face.

When data of one row (640dots) have been input, they will be latched in the form of parallel data for 640 lines of signal electrodes by latch signal CP1. Then the corresponding drive signal will be transmitted to the 640 lines of column electrodes of the LCD panel by the LCD drive circuits.

At this time, scan start-up signal S has been transferred from the scan signal driver to the 1st row of scan electrodes, and the contents of the data signals are displayed on the 1st rows of upper and lower half of the display face according to the combinations of voltages applied to the scan and signal electrodes of the LCD

While the 1st rows of data are being displayed, the 2nd rows of data are entered When 640 dots of data have been transferred then latched on the falling edge of CP1 clock, the display face proceeds to the 2nd rows of display.

Such data input will be repeated up to the 240th row of each display segment, from upper to lower rows, to complete one frame of display by time sharing method. The data input proceeds to the next display face.

Scan start-up signal S generates scan signal to drive horizontal electrodes.

Since DC voltage, if applied to LCD panel, causes chemical reaction which wil deteriorate LCD panel, drive waveform shall be inverted at every display frame to prevent the generation of such DC voltage. Control Signal M plays such role.

Because of the characteristics of the CMOS driver LSI, the power consumption of the Module goes up as the operating frequency CP2 increases. Thus the driver LSI applies the system of transferring 4-bits parallel data through the 4 lines of shift registers to reduce the data transfer speed CP2. Thanks to the LSI, the power consumption of the Module will be minimized.

.

In this circuit configuration, 4-bit display data shall be therefore input to data input pins of DU_{0-3}(upper display segment) and DL_{0-3}(lower display segment).

Furthermore the LCD Module adopts bus line system for data input to minimize the power consumption. In this system data input terminal of each driver LSI activated only when relevant data input is fed.

Data input for column electrodes of both the upper and the lower display segment and chip select of driver LSI are made as follows:

The driver LSI at the left end of the display face is first selected, and the adjacent driver LSI of the right side is selected when 80 dots data (20CP2) is fed. This process is sequentially continued until data is fed to the driver LSI at the right end of the display face.

This process is simultaneously followed at the column drivers LSI's of both the upper and the lower display segments. Thus data input for both the upper and the lower display segments must be fed through 4-bit bus line sequentially from the left end of the display face.

Since this graphic display Module contains no reflesh RAM, it requires data and timing pulse inputs even for static display.

The timing chart of input signals are shown in Fig. 3 and Table 7.

7. Optical Characteristics $Ta=25\ ^{\circ}C, V_{DD}-V_{EE}=Vmax$

Table 8

Following spec are based upon the electrical ❑ easuring conditions, on which the contrast of perpendicular direction ($\theta x=\theta y=0$ ") will be MAX.

Parameter		Symbol	Condition	MIN.	TYP.	MAX.	Unit	Remark
Viewing angle range		θx	Co > 4.0 ey=o "	-25	-	25	dgr.	Note 1
		θy	ex=o °	-lo	-	20	dgr.	
Contrast ratio		co	$\theta x=\theta y=0$ "	10	**18**	-	-	**Note** 2
Response time	Rise	τr	$\theta x=\theta y=0$ °	-	200	300	ms	Note 3
	Decay	τd	$\theta x=\theta y=0$ o	-	150	250	ms	

Note 1) The viewing angle range is defined as shown Fig. 4.

Note 2) Contrast ratio is defined as follows:

$$Co = \frac{\text{Luminance(brightness) all pixels 'white" at Vmax}}{\text{Luminance(brightness) all p. xels "dark" at Vmax}}$$

Vmax is defined in Fig. 6.

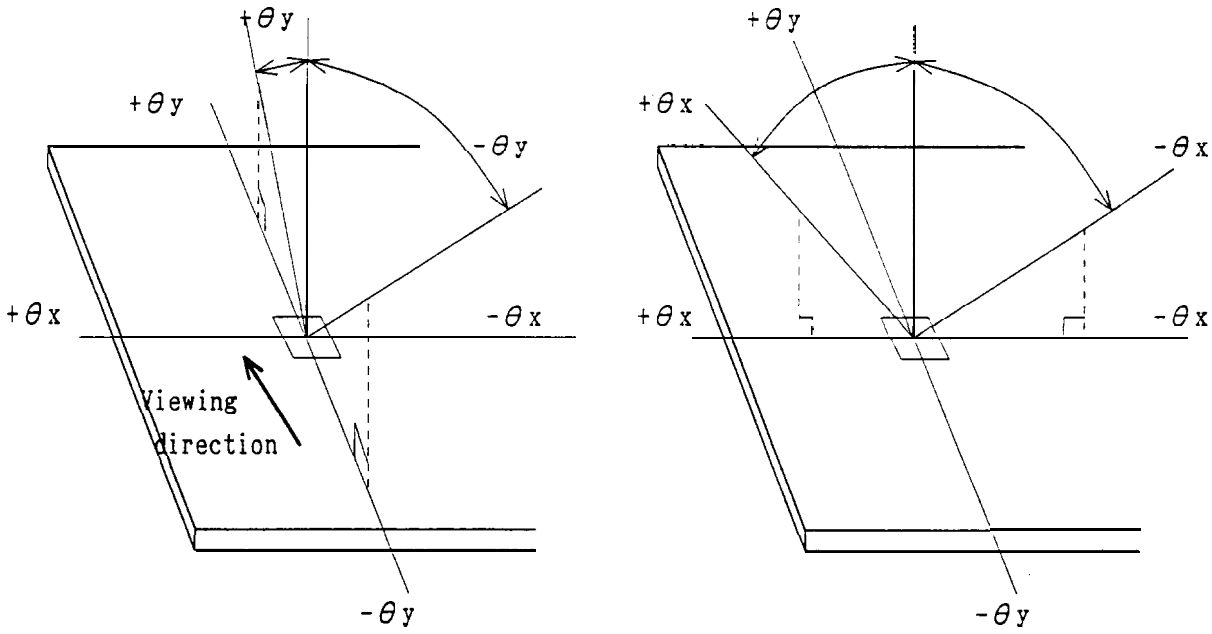
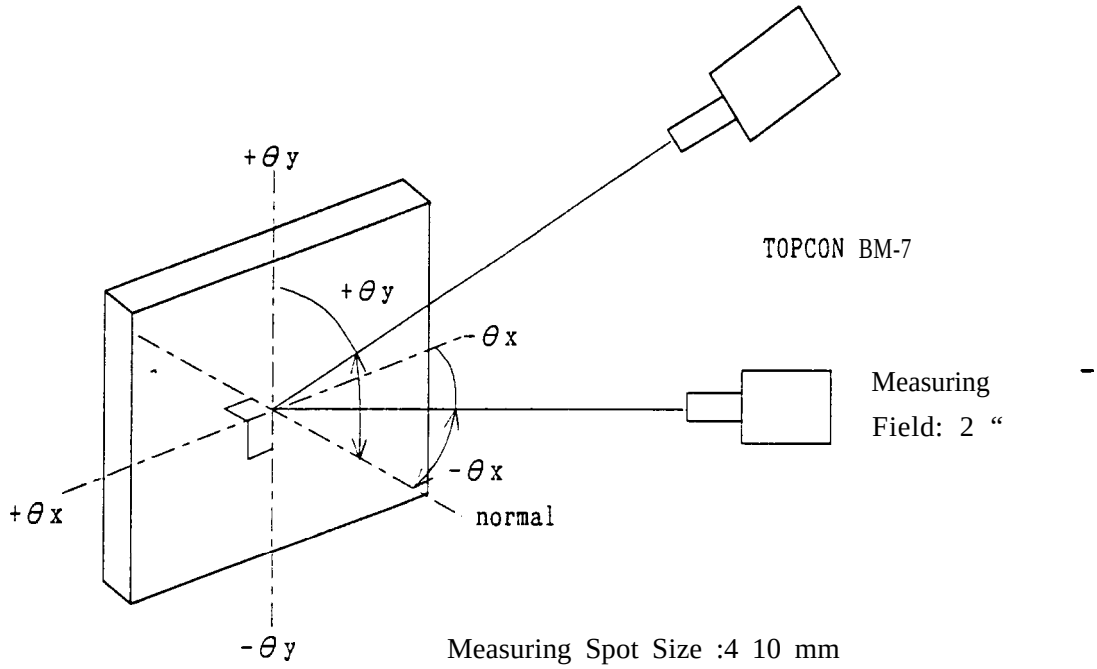


Fig. 4 Definition of Viewing Angle

Note 3) The response characteristics of photo-detector output are measured as shown in Fig.7, assuming that input signals are applied so as to select and deselect the dots to be measured, in the optical characteristics test method shown in Fig.8.



Measuring Spot Size :4 10 mm

θx : Angle from “normal”to viewing surface rotated about the horizontal axis.

θy : Angle from “normal”to viewing surface rotated about the vertical axis.

Fig.5 Optical Characteristics Test Method I

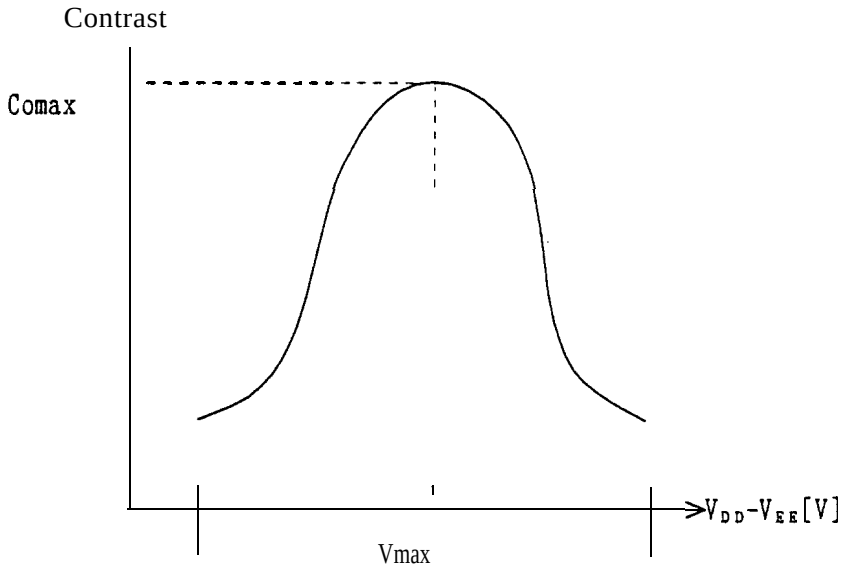


Fig.6 Definition of Vmax

(Response Measurement)

Memory Scope

TEKTRONIX
TYPE549
STORAGE
OSCILLOSCOPE

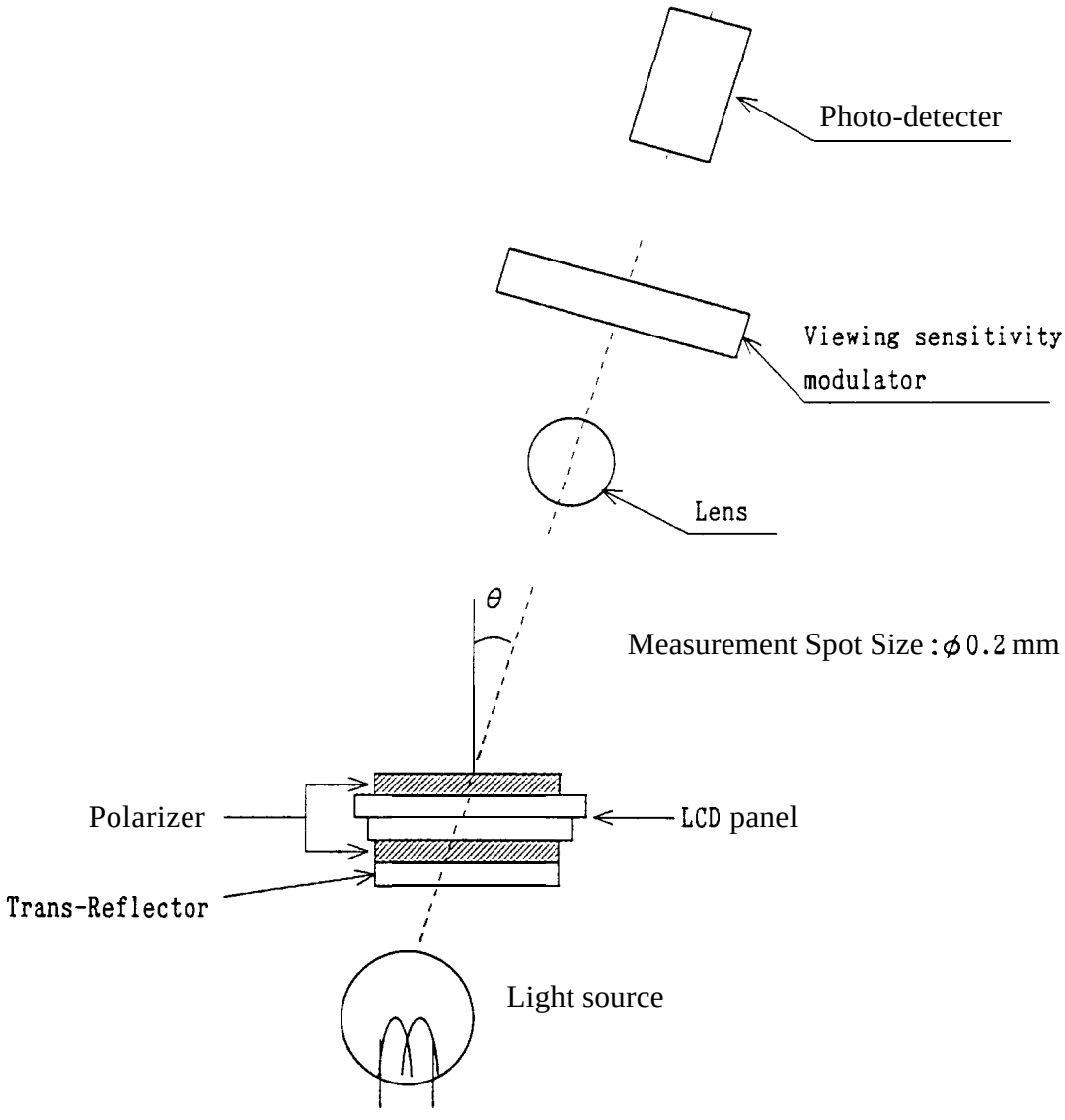


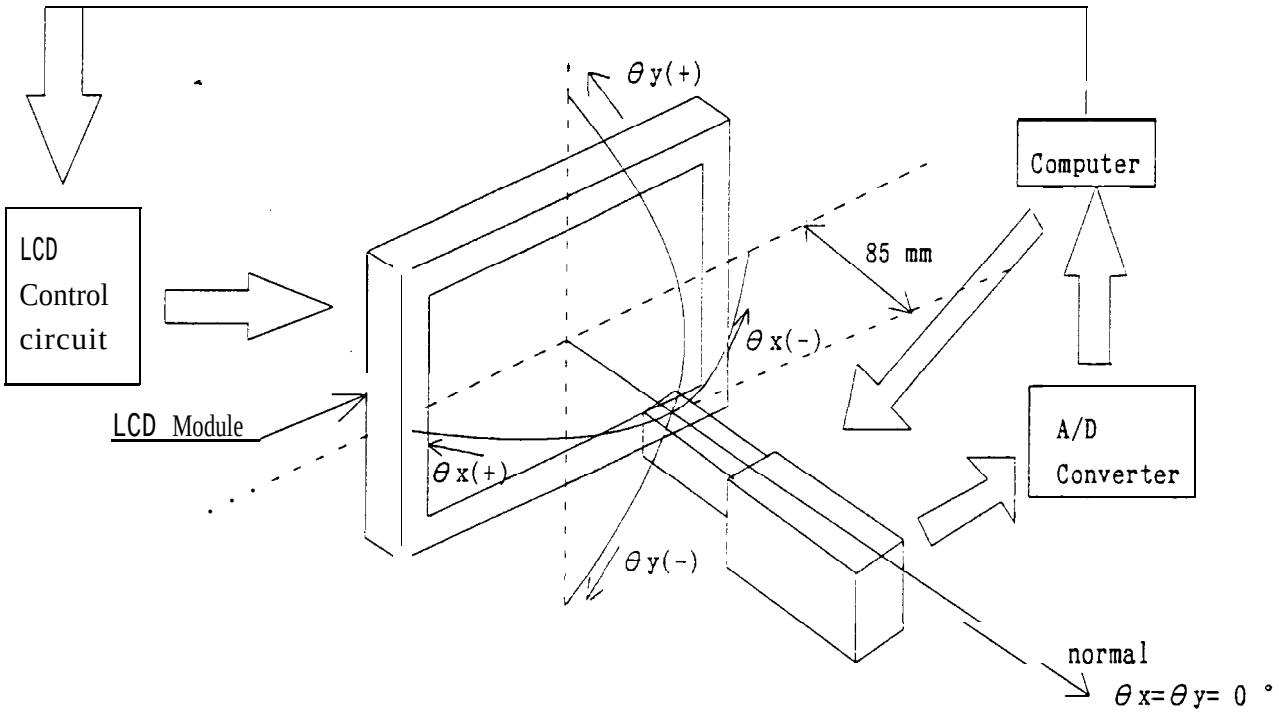
Fig.7-1 Optical Characteristics Test Method II

(Transmissive mode)

(Response Measurement)

Ta=25 "C

In dark room



TOPCON BM7 + quartz fiber

(Measurirg Spot Size: ϕ 10.. ,

Measuring Field: 2 ")

Fig.7-3 Optical Characteristics Test Method II

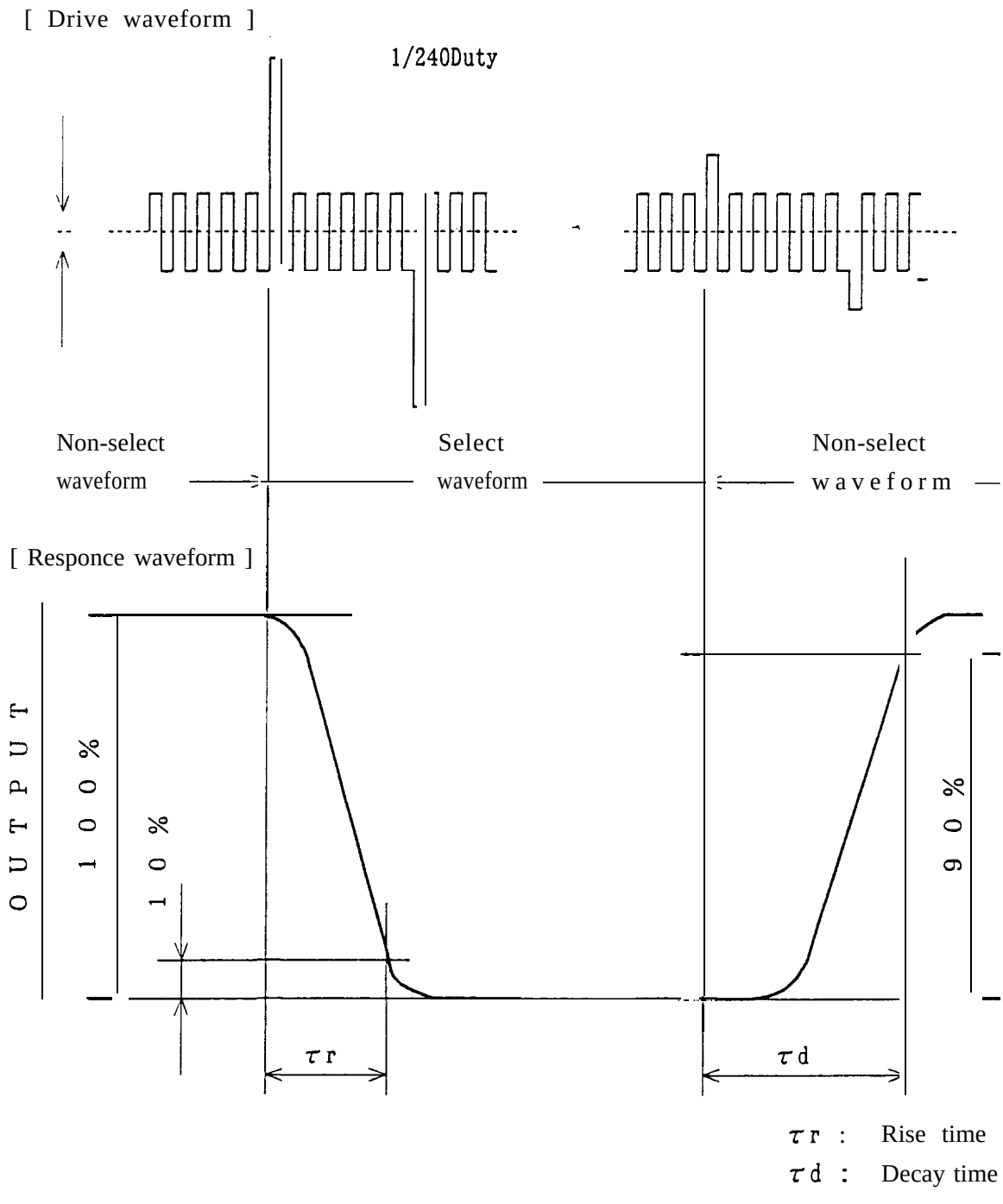
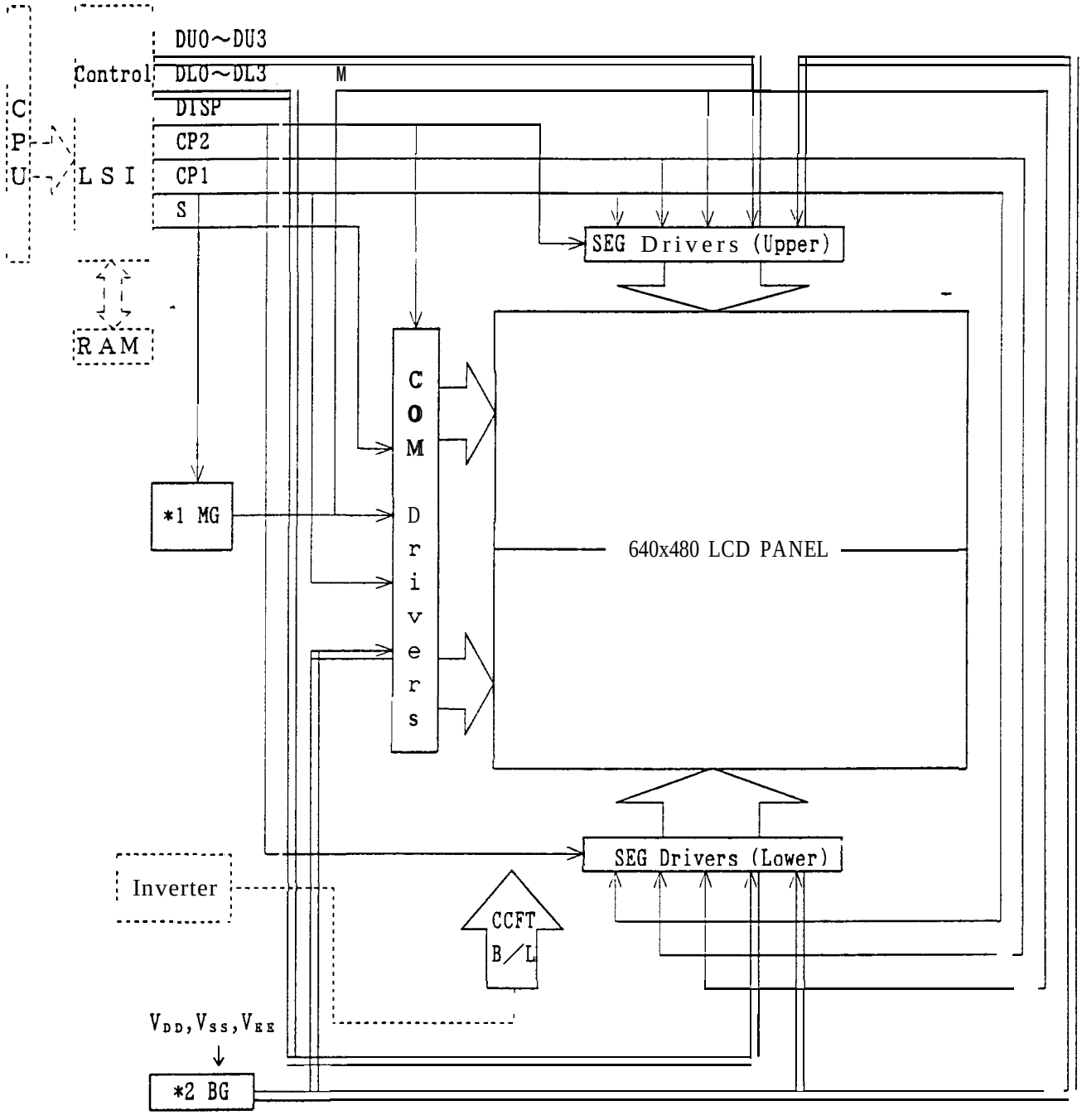


Fig.8 Definition of Response Time



*1 MG: M GENERATOR CIRCUIT

*2 BG: BIAS GENERATOR CIRCUIT

Fig.9 Circuit block diagram

出図 ISSUE
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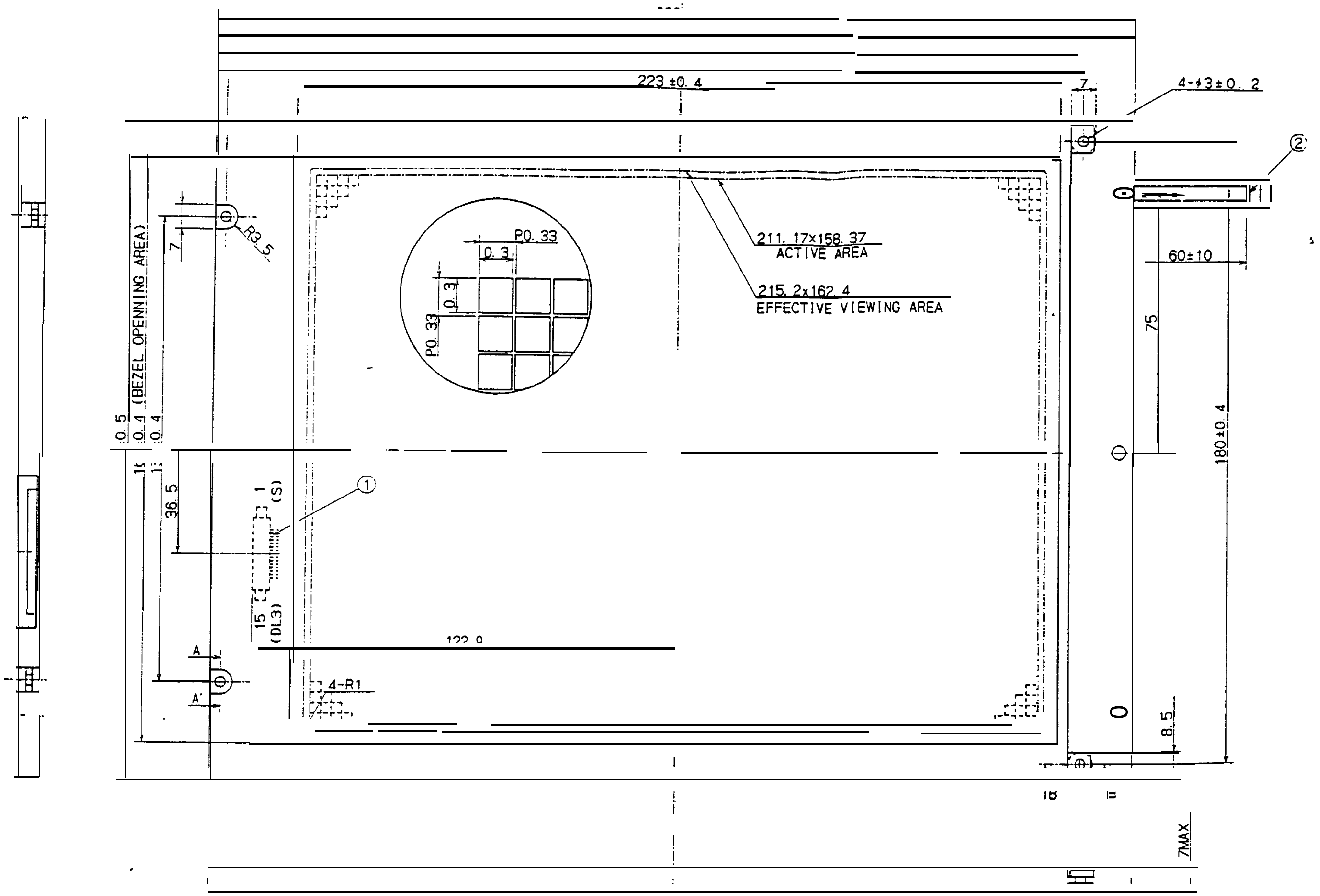
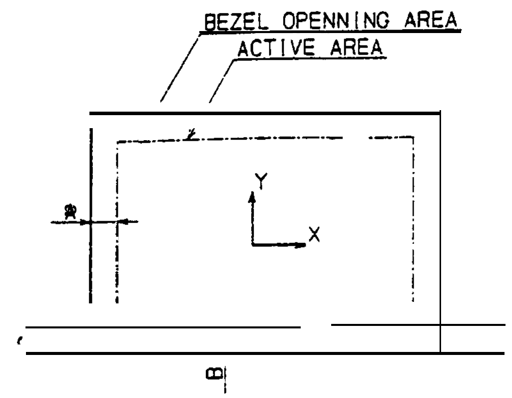
新設 NEW · 変更 CHANGE · 書換 REPLACE 図面



BEZEL/DISPLAY POSITION



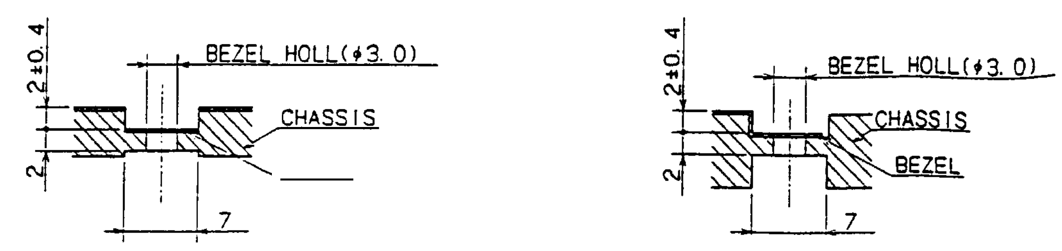
1 TOL(TOLERANCE)X-direction A:5.9±0.8
2 TOL(TOLERANCE)Y-direction B:5.3±0.8
3 OBLIQUITY of DISPLAY AREA IC-DI<0.8

1 INTERFACE CONNECTOR(15pins)
SD-53261-1510 (MOLEX)

2 CCFT CONNECTOR
M63M83-04 (MITSUMI)

INTERFACE PIN LAYOUT

PIN#	1	2	3	4	5	6	7	8
Symbol	S	CP1	CP2	DISP	VDD	VSS	VEE	DU0
PIN#	9	10	11	12	13	14	15	
Symbol	DU1	DU2	DU3	DL0	DL1	DL2	DL3	



A-A' SECT

B-B' SECT

指示なき寸法公差は ±0.5 とする UNSPECIFIED TOL TO BE

名称 NAME	640X480Dots 0.33Pitch LCD UNIT OUTLINE DIMENSIONS
適用機種 MODEL	LM64P89L / LM64P89
年月日 DATE	
改定記事 RIVISE	
材質 MATERIAL	
板厚 THIKNESS	
仕上 FINISH	
尺度 SCALE	
記号 SYMBOL	
部品コード PARTS CODE	
作成日付 DATE	1993 · 7 · 5
図番 DRAWING No	

設計 DESIGN | 製図 TRACE | 検図 | 検図 | 承認 APPROVE

SHARP CORPORATION
シャープ株式会社 液晶（事本）
発行部門 NEW B/W LCD PLT

8. Characteristics of Backlight

The ratings are given on condition that the following conditions are satisfied.

1) Rating(NOTE)

Parameter	Min	Typ	Max	Unit
Brightness	60	75	-	cd/m²

2) Measurement circuit : LMOOOI06(SHARP) (at IL=5 mArms)

3) Measurement equipment: BM-7 (' OPCON

4) Measurement conditions

4-1 Measurement circuit voltage: DC=12 V at primary side

4-2 LCD: All digits WHITE, VDD=5 V, VDD-VEE=Vmax, DUO～DU3

(refer Fig.6 DLO～DL3="L" (WHITE)

4-3 Ambient temperature: 25 "C

Measurement shall be executed 30 minutes after turning on.

5) Used lamp: HMBS3D87W180NLS/AXZ

5-1 Ratings(1pc)

I Parameter		Max. allowable value
Circuit voltage(VS)	1000 Vrms MIN	1500 Vrms
Discharging tube current	5 mArms TYP	6 mArms *
Power comsumption	2.1 W	—
Discharging tube voltage	500 Vrms TYP	-
Brightness(B)	32500 cd/m² TYP	-

Within no conductor closed.

* It is recommended that IL be not more than 5 mArms so that heat radiation of CCFT backlight may least affect the display quality.

5-2 Operating life time

Parameter	Min.	Typ.	Max.	Unit	Conditions
operating life time	15 000	25 000	-	hours	IL= 5 mArms

(CCFT invecter LM000106 or equivalent)

The inverter should meet the following conditions;
-Sine, symmetric waveform without spike in positive and negative.

–The voltage at the secondary side is 1,000 Vrms or more.
-Illuminance frequency is from 25kHz to 45kHz.

The operating life time is defined as having ended when any of the following conditioned occur; (25±5 'C)
-When the voltage required for initial discharge has reached 980 Vrms or when it has reached 10.8 V-DC when used an inverter.
-When the illuminence or quantity of light has decreased to 50 % of the initial value.

NOTE) Rating are defined as the average brightness inside the viewing area specified in Fig.11.

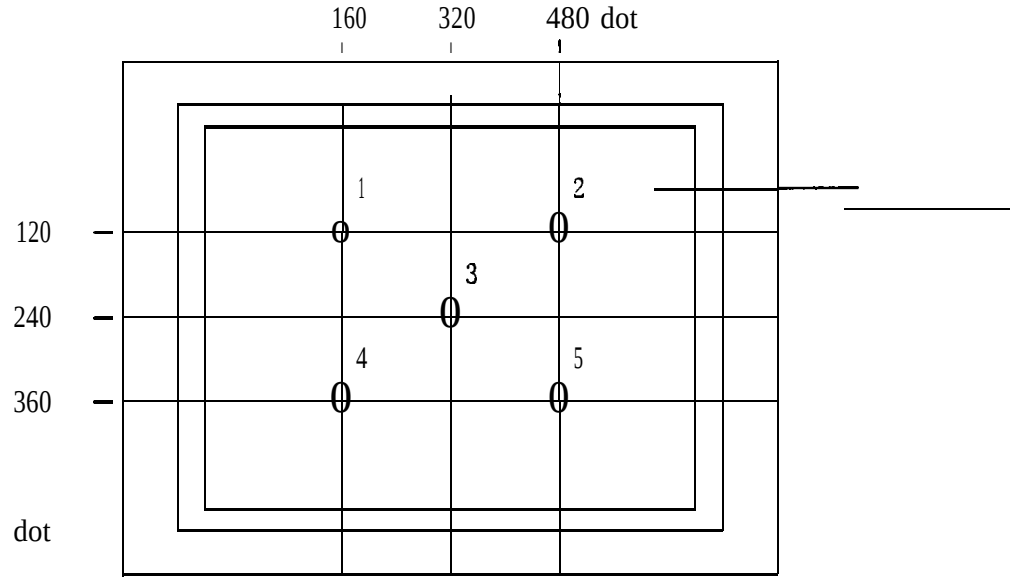


Fig.11 Measuring points(1~5)

9. Precautions

1)Industrial(Mechanical)design of the product in which this LCD Module will be incorporated must be so made that the viewing angle characteristics of the LCD maybe optimized.

This Module's viewing angle is illustrated in Fig.12.

$\theta y\min <$ viewing angle $< \theta y\max$ ($\theta y\min < 0$ " $\theta y\max \geqq 0^{0}$)

(For the specific values of $\theta y\min, \theta y\max$, refer to the table 8.)

Please consider the optimum viewing conditions according to the purpose when installing the Module.

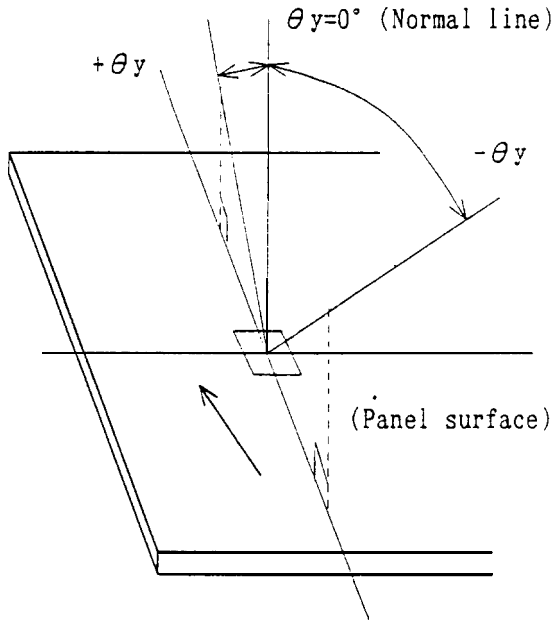


Fig.12 Dot matrix LCD viewing angle

2) This Module is installed using mounting tabs at the four corners of PCB or bezel.

When installing the unit, pay attention and handle carefully not to allow any undue stress such as twist or bend.

A transparent acrylic resin board or other type of protective panel should be attached to the front of the Module to protect the polarizer, LCD cells,etc.

3) Since the front polarizer is easily damaged, please pay attention not to scratch on its face.

4) If the surface of the LCD cells needs to be cleaned, wipe it swiftly with cotton or other soft cloth. If still not completely clear, blow on its and wipe.

5) Water droplets, etc. must be wiped off immediately since they may cause color changes, staining, etc. if remained for a long time.

6) Since LCD is made of glass plates, dropping the Module or banging it against hard objects may cause cracking or fragmentation.

7) CMOS LSIS are equipped in this Module, so care must be taken to avoid the electro-static charge, by earthing human body, etc. Take the following measures, to protect the unit from the electric discharge via mounting tabs from the main system the electrified with static electricity.

(1) Earth the metallic case of the main system (contact of the unit and main system).

(2) Insulate the Module and main system by attaching insulating washers made of bakelite or nylon, etc.

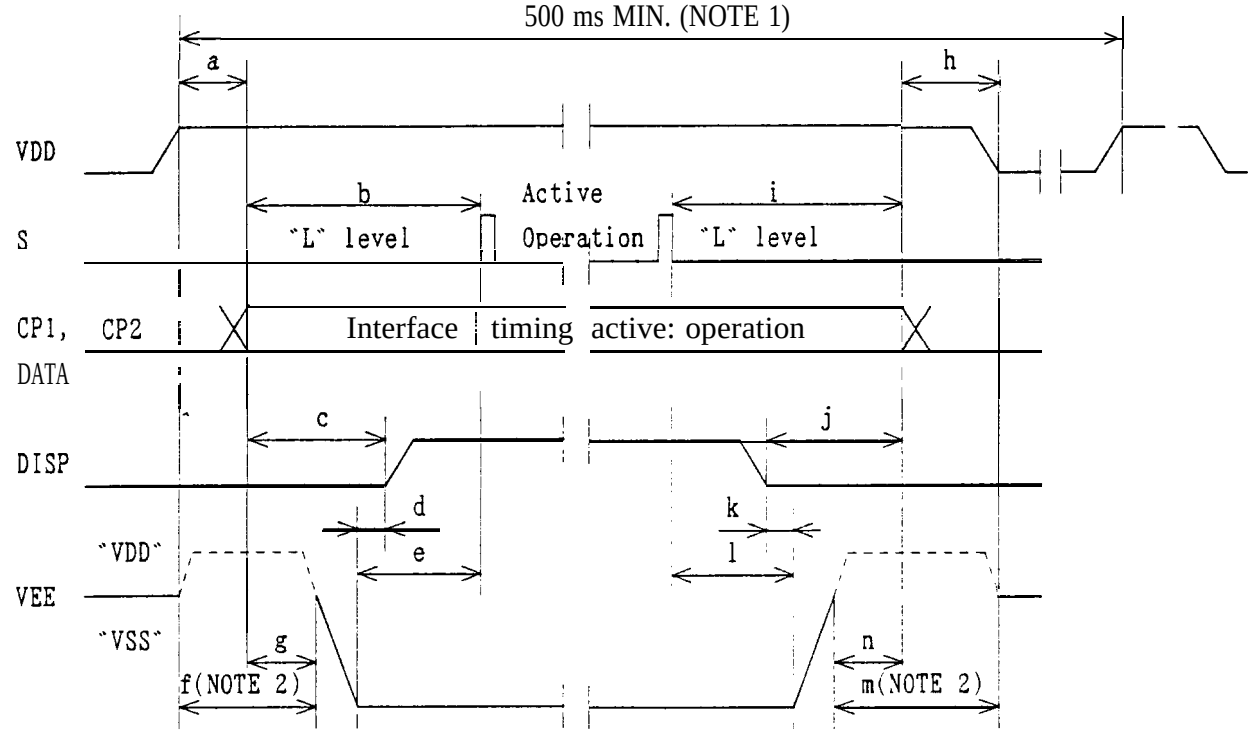
8) The Modele should be driven according to the specified ratings to avoid malfunction of parmanent damage. DC voltage drive leads to rapid deterioration of LC, so ensure that the drive is alternating waveform by continous application of the signal M. Especially the power ON/OFF sequence shown on next page shall be followed to avoid latch-up of driver LSIS and application of DC voltage to LCD panel.

9) Avoid to expose the Module to the direct sun-light, strong ultra-violet light, etc. for a long time.

10) If stored at temperatures below specified storage temperature, the LC may freeze and be deteriorated. If storage temperature exceed the specified rating, the molecular orientation of the LC may change to that of a liquid, and they may not return to their original state.

11) Disassembling the LCD Module can cause permanent damege and should be strictly avoided.

Supply voltage sequence condition



POWER ON			POWER OFF		
SYMBOL	With DISP control	Without DISP control	SYMBOL	With DISP control	Without DISP control
a	O ms MIN.	O ms MIN. 20 ms MAX.	h	O ms MIN.	O ms MIN. 20 ms MAX.
b	O ms MIN.	20 ms MIN.	i	O ms MIN.	20 ms MIN.
c	20 ms MIN.		j	20 ms MIN.	
d	Oms MIN.		k	O ms MIN.	
e		O ms MIN.	l		0 ms MIN.
f	O ms MIN.	(NOTE2)	m	O ms MIN.	(NOTE2)
g		O ms MIN. 100 ms MAX.	n		100 ms MIN.

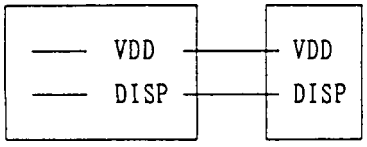
(NOTE 1) Power ON/OFF cycle time. All signals and power line shall be in accordance with above sequence in case of power ON/OFF.

(NOTE 2) VEE to be set at "VDD level" or "open". VEE should be in accordance with the dotted line when DISP(display control signal) is not used.

(NOTE 3) Connection of DISP (pin. No.4)

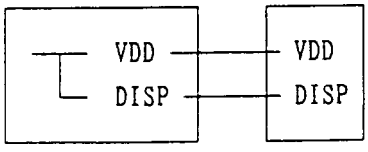
○With DISP control

Input DISP control signal shown on this page.



OWithout DISP control

DISP to be connected with VDD.



10. Lot number

Lot number is shown at the position mentioned in Fig.13 in accordance with the following numbering rule.

(Example)

96 B 00001 ( )

- ( ) — Factory Identification Code. (Alphabet)
- 00001 — Serial number(Missing number exist)
- B — Production month (A= JAN., B=FEB.,···L=DEC.)
- 96 — Production year

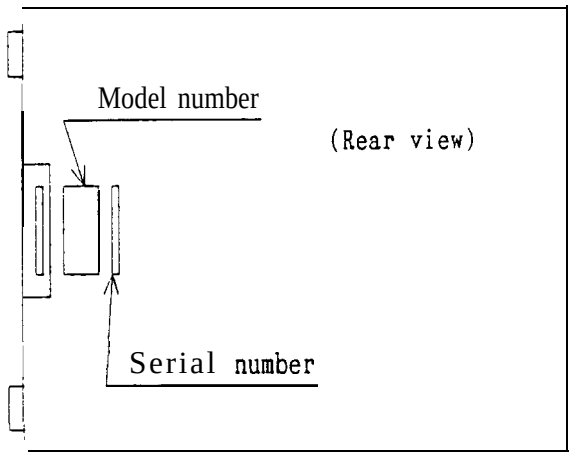


Fig.13

11. Applicable inspection standard

The LCD Module shall meet the following inspection standard
: S-U-012 -01

12. This specification describes display quality in case of no gray scale. Since display quality can be affectedly gray scale methods, display quality shall be carefully evaluated for the usability of the LCD Module in case gray scale is displayed on the LCD Module.

WARNING

DON' T USE ANY MATERIALS WHICH EMIT GAS FROM EPOXY RESIN (AMINES' HARDENER) AND SILICONE ADHESIVE AGENT (DEALCOHOL OR DEOXYM) TO PREVENT CHANGE POLARIZER COLOR OWING TO GAS.